IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A power monitor circuit operable to notify processing circuits operating from a first power supply having a VDD output voltage when a second power supply having a VDDIO output voltage is powered up, wherein VDDIO is greater than VDD, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

~~an odd number of serially connected~~ one or more inverters operating from said first power supply, said one or more inverters comprising an odd number of serially connected inverters, wherein an input of ~~a first~~ one of said one or more ~~serially connected~~ inverters is connected to said voltage divider circuit output node and an output of ~~a last~~ one of said one or more ~~serially connected~~ inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

2. (Currently Amended) The power monitor circuit as set forth in Claim 1 wherein said one or more serially connected inverters comprise one or more CMOS inverters.

3. (Original) The power monitor circuit as set forth in Claim 1 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

4. (Original) The power monitor circuit as set forth in Claim 3 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

5. (Original) The power monitor circuit as set forth in Claim 4 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

6. (Original) The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises one inverter.

7. (Original) The power monitor circuit as set forth in Claim 6 wherein said odd number of serially connected inverters comprises one CMOS inverter.

8. (Original) The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises three inverters.

9. (Original) The power monitor circuit as set forth in Claim 8 wherein said odd number of serially connected inverters comprises three CMOS inverters.

10. (Original) The power monitor circuit as set forth in Claim 1 wherein said odd number of serially connected inverters comprises five inverters.

11. (Original) The power monitor circuit as set forth in Claim 10 wherein said odd number of serially connected inverters comprises five CMOS inverters.

12. (Currently Amended) An integrated circuit comprising:

core processing circuitry operating from a first power supply having a VDD output voltage;

output stage circuitry operating from a second power supply having a VDDIO output voltage, wherein VDDIO is greater than VDD; and

a power monitor circuit operable to notify said core processing circuitry when said second power supply having said VDDIO output voltage is powered up, said power monitor circuit comprising:

a voltage divider circuit coupled between said second power supply and ground and having an output node that rises to a high voltage when said second power supply is powered up; and

~~an odd number of serially connected~~ one or more inverters operating from said first power supply, said one or more inverters comprising an odd number of serially connected inverters, wherein an input of ~~a first~~ one of said one or more ~~serially connected~~ inverters is connected to said voltage divider circuit output node and an output of ~~a last~~ one of said one or more ~~serially connected~~ inverters produces a status signal that is low when said voltage divider circuit output node is high and is high when said voltage divider circuit output node is low, and wherein said status signal is an input signal to said voltage divider circuit operable to minimize DC current consumption in said voltage divider circuit when said second power supply is powered up while maintaining a value of said status signal.

13. (Currently Amended) The integrated circuit as set forth in Claim 12 wherein said one or more serially connected inverters comprise one or more CMOS inverters.

14. (Original) The integrated circuit as set forth in Claim 12 wherein said voltage divider circuit comprises: 1) a first N-channel transistor having a gate and a drain coupled to said VDDIO output voltage and a source coupled to said voltage divider circuit output node; 2) a second N-channel transistor having a gate coupled to said VDD output voltage and a drain coupled to said voltage divider circuit output node; and 3) a third N-channel transistor having a gate coupled to said status signal, a drain coupled to a source of said second N-channel transistor, and a source coupled to ground.

15. (Original) The integrated circuit as set forth in Claim 14 further comprising a capacitor coupled between said voltage divider circuit output node and ground.

16. (Original) The integrated circuit as set forth in Claim 15 further comprising a fourth N-channel transistor having a gate coupled to said VDD output voltage, a drain coupled to said VDDIO output voltage, and a source coupled to said voltage divider circuit output node.

17. (Original) The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises one inverter.

18. (Original) The integrated circuit as set forth in Claim 17 wherein said odd number of serially connected inverters comprises one CMOS inverter.

19. (Original) The integrated circuit as set forth in Claim 12 wherein said odd number of serially connected inverters comprises three inverters.

20. (Original) The integrated circuit as set forth in Claim 19 wherein said odd number of serially connected inverters comprises three CMOS inverters.

21. (Original) The integrated circuit as set forth in Claim 20 wherein said odd number of serially connected inverters comprises five inverters.

22. (Original) The integrated circuit as set forth in Claim 21 wherein said odd number of serially connected inverters comprises five CMOS inverters.